St. Petersburg State University of Aerospace Instrumentation

SUAI

Department of aerospace computer and software systems

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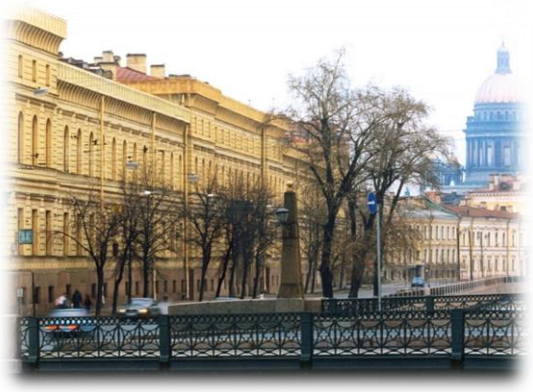


Department of aerospace computer and software systems

Bachelor of engineering and technology (4 years)

- Automated data processing and control systems
- Integrated automated information systems
- Information science and computing systems

Master of engineering and technology (2 years)

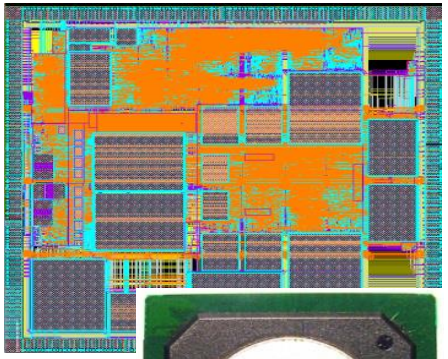
- Embedded data processing and control systems

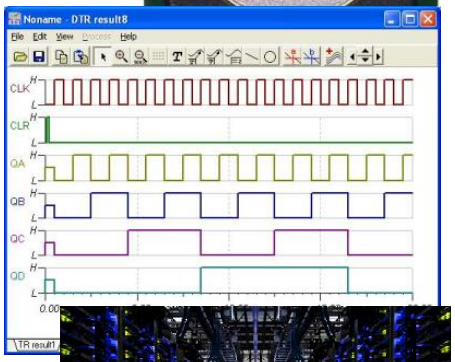
Chairs head: Yuriy Sheynin, professor, doctor of science

Chair stuff		**Chair students**	
Professors	6	Bachelor	200
Associate prof.	12	Master	20
Lecturers	4	PhD	8

Studying

- Processors, microprocessors, System-on-Chips, Network–on-Chips, Interfaces of embedded systems
- Embedded systems VLSI design, VHDL, specification and modeling languages (SDL, SystemC)
- Computing networks, telecommunications, network standards, Smart systems, Internet of things
- Industrial data processing and control systems
- High-performance and parallel data processing systems
- Theory of information and coding, systems of multimedia data compression and coding
- Real-time operating systems for embedded systems
- Digital image and signal processing





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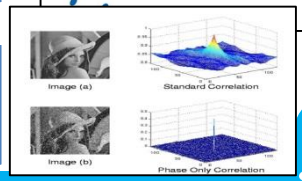


Implementation of CDIO at SUAI

CDIO is an innovative educational framework for producing the next generation of engineers.

Conceive – **D**esign

Implement – **O**perate

CDIO implementation for the «Embedded systems» program:

- Students study in respect to the CDIO standards, participate in joint multidisciplinary projects. These projects are supervised by the representatives of industrial partners.
- SUAI representative successfully passed the studies at "*CDIO Academy*";
- Updated the curricular according to CDIO standards and CDIO Syllabus;
- Chose the laboratories for CDIO studies;
- Developed the tasks for the projects.

More information: http://k14.spb.ru/

At 2015 SUAI officially became a member of CDIO Community (first University in St. Petersburg and 13th in Russia).

Students study, make projects, HW/SW design and system integration

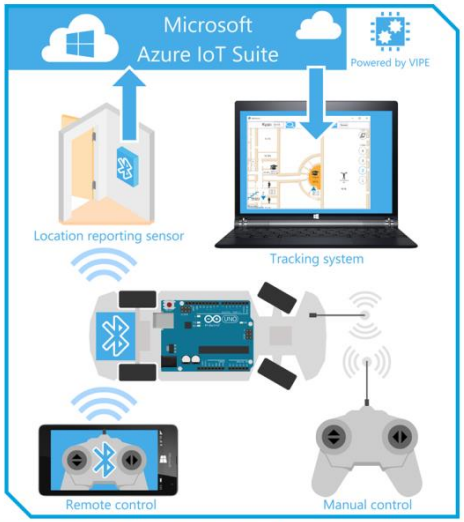
Saint-Petersburg State University of Aerospace Instrumentation

Arduino Based Automated Vehicle Multifunctional Platform.

Student project

Best Project - Europe

"Live Hard, Ship Hard!" is a student project aimed to make an automated Arduino based vehicle and to use Azure **IoT** Suite.
The project was for the "World's Largest Arduino Maker Challenge" competition and has won the "Best Project – Europe" prize.



- Smart line tracking. Automatically return to the path
- Providing location and automated vehicle platform data using via Bluetooth by using Azure IoT Suite
- Using the SUAI buildings navigation system for the vehicle tracking
- Remote control by Windows Phone smartphone via Bluetooth
- Partial use of visual programming in VIPE (Visual Programming Environment)

Scan to see more (videos + full description):

www.hackster.io/challenges/arduino-microsoft-maker

Project name	"Live Hard, Ship Hard!"
Project type	Cyber-physical system
Students level	bachelor
Team	• 2-3 students • 1 month
Activities	• soldering • prototyping • programming • 3D printing
Challenge name	World's Largest Arduino Maker Challenge
Status	"Best Project - Europe" award

hackster.io

Arduino

Microsoft

Russia, St. Petersburg,
Bolshaya Morskaia st. 67
Phone: +7 (812) 571-15-22

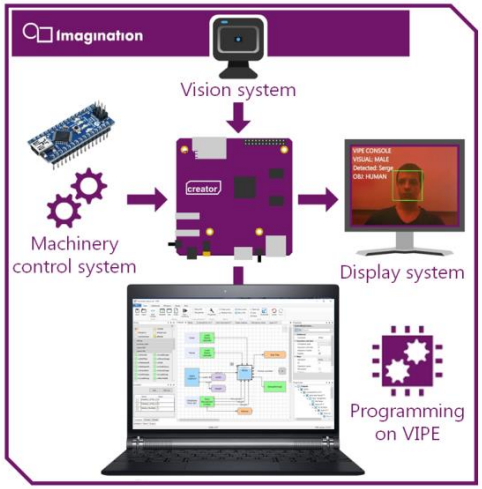
Yuriy E. Sheynin
Head of the Aerospace Computer and Software Systems Department
Telephone: +7 (812) 710-65-39

Saint-Petersburg State University of Aerospace Instrumentation

Terminator Vision System.

Student project

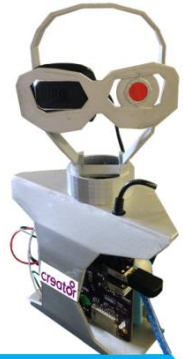
The "Terminator Vision System" is a student project aimed to make complex Autonomous Cyber-Physical System combining multicore computations, control and mechanical parts. The Vision System identifies people from the database and tracks them with rotating camera.
System is based on the Imagination Ci-20 Creator board with a heterogeneous multicore SoC .
This project is a part of "Creator Ci20 Terminator Challenge" world competition.



- Project is developed with the advanced visual multicore programming tool VIPE (Visual Programming Environment)
- Face recognition is performed by using training neural network
- Database of faces was created for face classification
- Tracking is performed by using servo, which is controlled by Arduino that receives commands from the Ci-20 bard

Scan to see more (videos + full description):

www.hackster.io/challenges/CI20/projects



Project name	"Terminator Vision System"
Project type	Cyber-Physical System
Students level	master
Team	• 2-3 students • 1 month
Activities	• prototyping • programming • 3D printing
Challenge name	Creator Ci20 Terminator Challenge

hackster.io

creator
Ci-20 board

Imagination

Russia, St. Petersburg,
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Phone: +7 (812) 571-15-22

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Head of the Aerospace Computing and Software Sy
Telephone: +7 (812) 710-65-39

Institute of High-Performance Computer and Network Technologies

- **R&D laboratories**
  - Software Systems Lab
  - System-on-Chip Lab
  - Embedded Computing for Mobile Communications Lab

SUAI

Research projects and activities

Network protocols and communications

Development of the communication protocols

UniPro™, PIE (for *MIPI Alliance*) - protocols for mobile devices

- SystemC modeling
- SDL specification and verification
- Proposals for specifications

SpaceWire (*University of Dundee and ESA*) - data-handling network for spacecrafts

- SystemC modeling
- SDL specification and verification
- Proposals for specifications, review, analysis
- Participation in SpaceWire WG meetings, International SpaceWire Conferences

SpaceWire-RT (*7th Framework Program project*) - development of **SpaceFibre** protocol

- SystemC modeling
- SDL specification and verification
- SpaceFibre specification review and correction

Development of the draft version of Russian national standard **SpaceWire-RUS** in terms of National SpaceWire Workgroup.

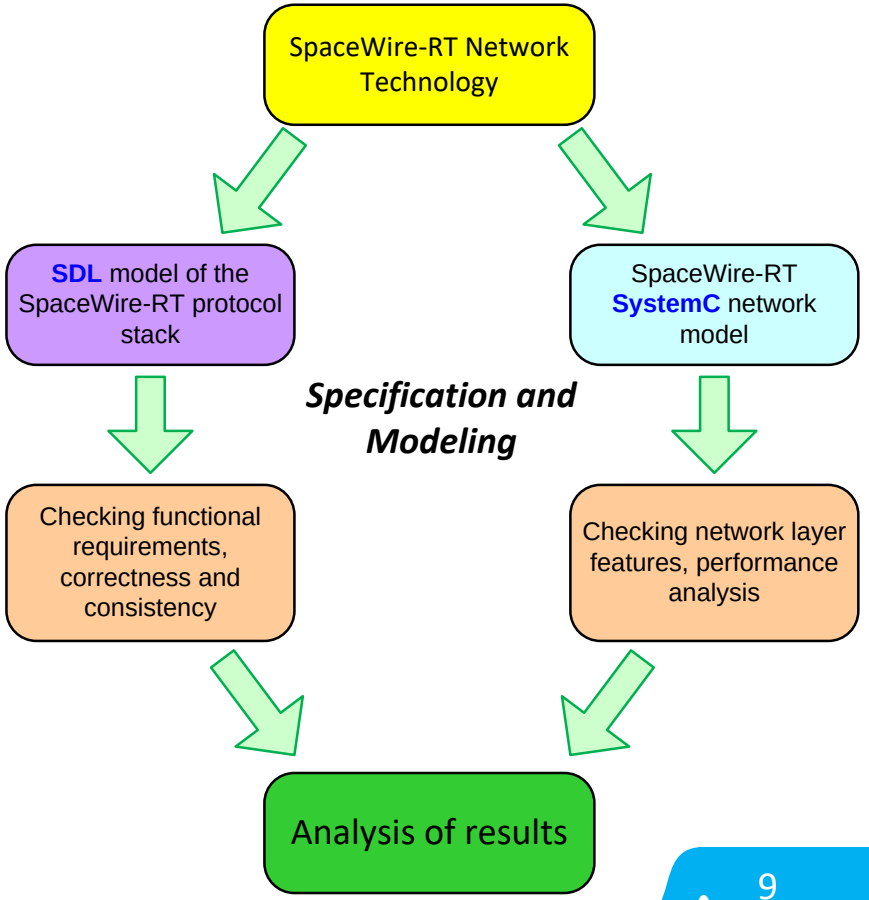
FP7 project “SpaceWire-RT” in EU-Russia Cooperation for Strengthening Space Foundations (SICA)

SUAI was a leading organization for two work packages:

- WP3: Spacewire-RT validation and simulation
- WP7: Exploitation and dissemination

Main impact:

- Definition of service access points for all layers of the protocol stack
- Proposal of changes to the quality of service mechanisms
- Proposal of the Management Layer position in the protocol stack, its functionality and responsibility
- Several major inconsistencies in the protocols mechanisms were found, which have been fixed in the SpaceFibre Draft F1 specification



STP-ISS protocol for SpaceWire on-board networks

Configuration flexibility: Different settings depending on the operation scenario.

Transport connections: Maximum 16 connections – 8 connections for one direction.

Flow control: for each transport connection.

Different implementation profiles: protocol has a list of mechanisms that are mandatory for the implementation, and others are additional.

User data types:

- Data messages
- Control commands
- System codes

Quality of service:

- Priorities
- Guaranteed delivery
- Non-guaranteed delivery
- Scheduling

Duplicate control commands detection

STP-ISS – a new transport protocol for the on-board equipment data exchange via the SpaceWire network. It is used for the continuous autonomous operation spacecraft of JSC academician Reshetnev's "Informational Satellite Systems". STP-ISS protocol has two revisions with different mechanisms and implementation profiles.

Software-to-Hardware tester for STP-ISS:

- Gives an ability for functional testing of onboard equipment with hardware or software implementation of STP-ISS protocol;
- Tester includes a laptop with the testing software and SpW USB Brick;
- The Device Under Test is connected with a tester by a SpaceWire connector.

Modeling of STP-ISS protocol (rev.1 and rev. 2):

- **C++ reference-code** – reference model of the protocol on C++;
- **SDL model** – intended for the clear formal description of the STP-ISS mechanisms.
- **Networking SystemC model** – gives an ability to test the networking functionality of STP-ISS on top of SpaceWire.

Two versions of IP-core is implemented for STP-ISS rev.1 and rev. 2.

Development of SpaceWire-Plug-and-Play technology for JSC «ISS»

Purposes:

- Reduce the time for the onboard networks development
- Reduce the time for onboard equipment testing
- Reduce the number of «human factor» errors for all stages of onboard network implementation
- Increase the reliability and fault tolerance
- Increase the modularity and scalability of onboard network

Network management includes:

- Network monitoring;
- Routing for the data streams;
- Network error recovery;
- Network security;
- Registration of new devices or software

Implemented the automatic construction of the onboard network with the initial technical details: node characteristics and data streams sizes.

The software for the implementation of the network nodes parameters is under development: transmission speed, logical addresses, routing table and so on…

Implemented the software to detect the place of the network manager.

Under the development the software module, that implements the algorithms for automatic setting of network structures.

Under the development the experimental software for the automatic setting of the network elements.

Under the development the experimental software for the automatic setting of the whole network.

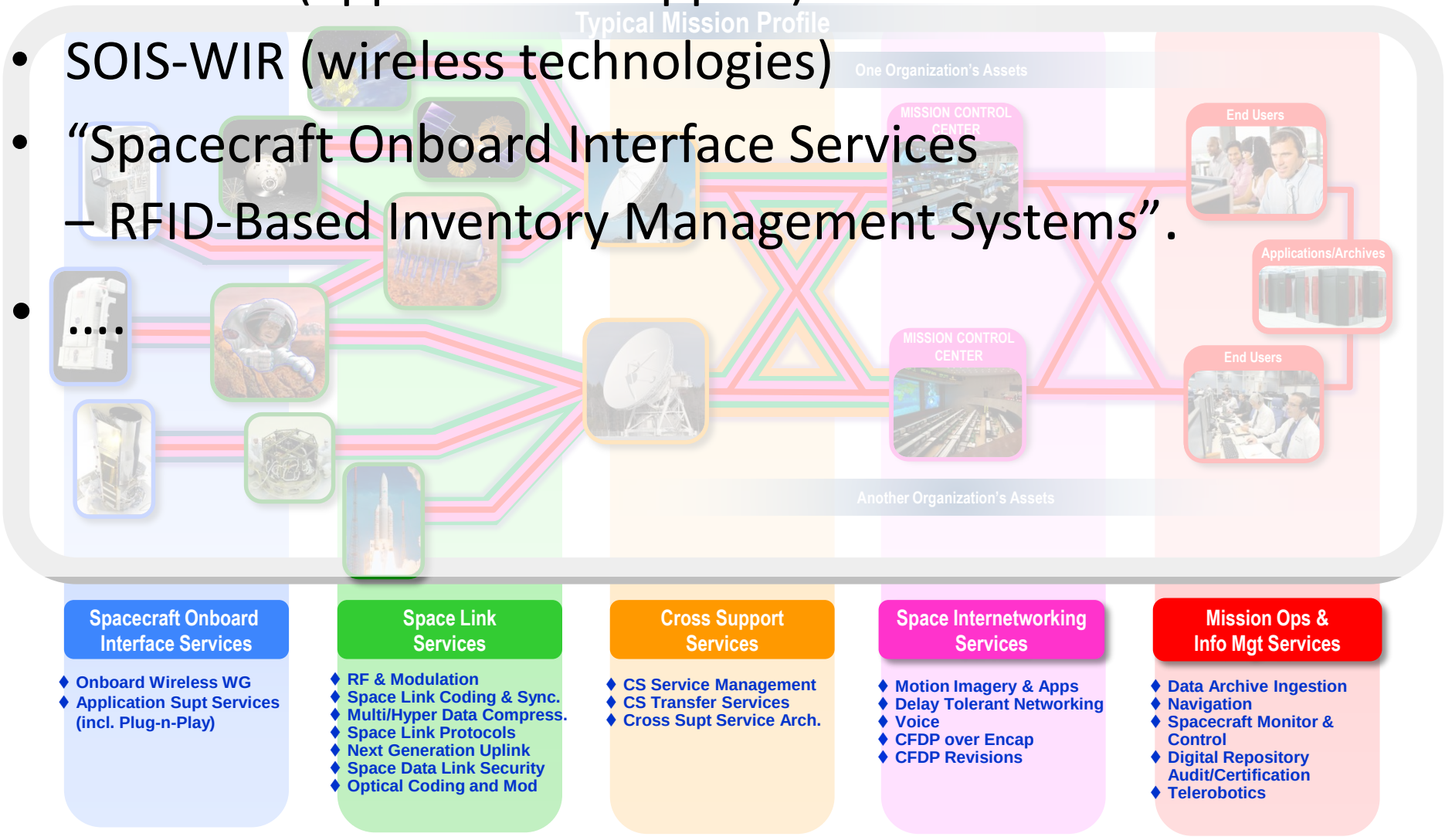
Development of the software complex for the design of the structure and logical setup of automatically settable distributed network structures, operating by SpaceWire-Plug-and-Play mechanisms.

Development of the software module, implementing algorithms for automatic setting of network structures, operating by SpaceWire-Plug-and-Play mechanisms

Development of the experimental software for the automatic setting of the network elements and the whole networks, operating by SpaceWire-Plug-and-Play mechanisms.

Collaboration within CCSDS

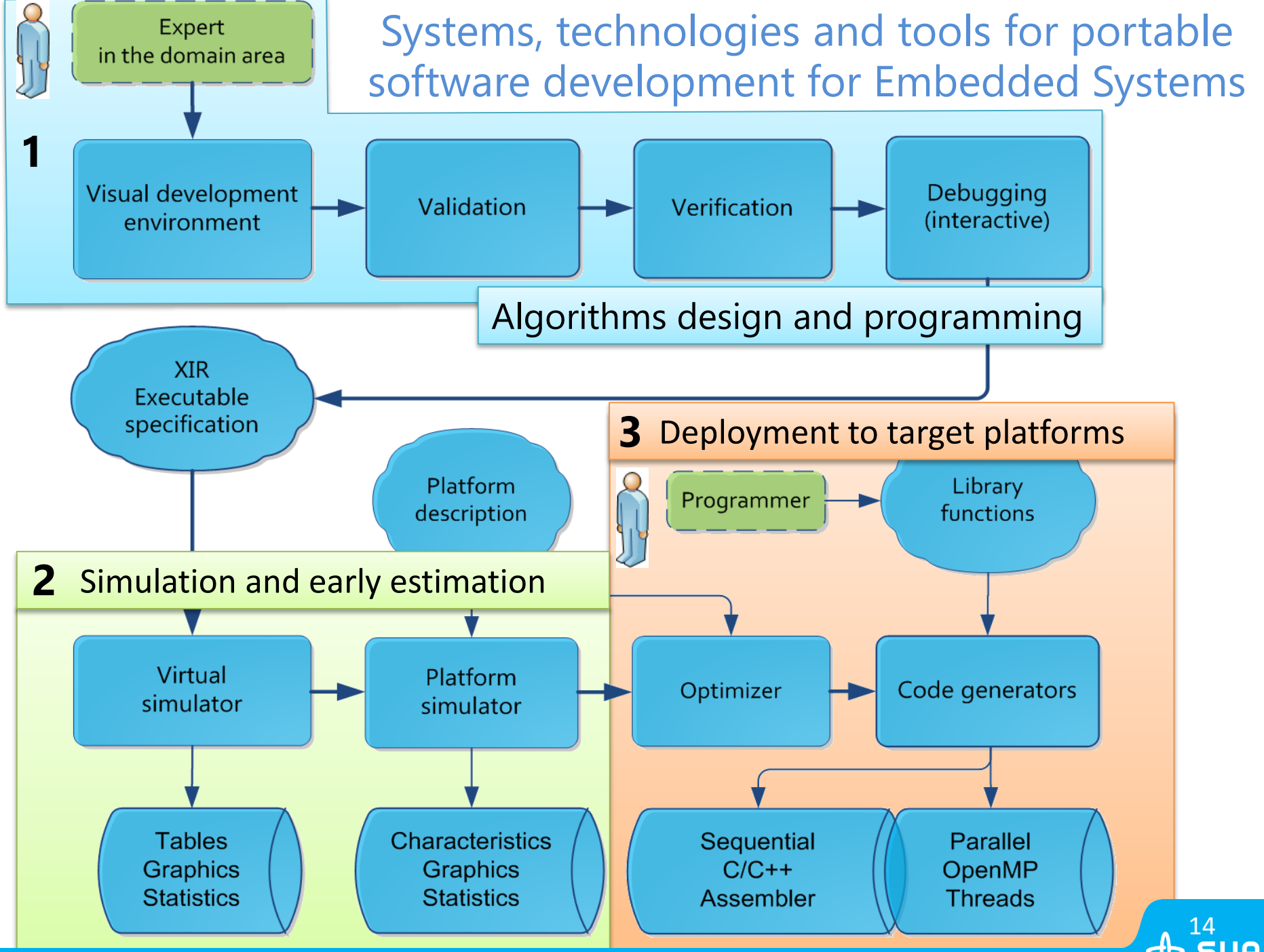
- SOIS-SOIF (network interfaces and services)
- SOIS-APP (applications support)
- SOIS-WIR (wireless technologies)
- “Spacecraft Onboard Interface Services – RFID-Based Inventory Management Systems”.
- ….



Research projects and activities

Software and hardware development

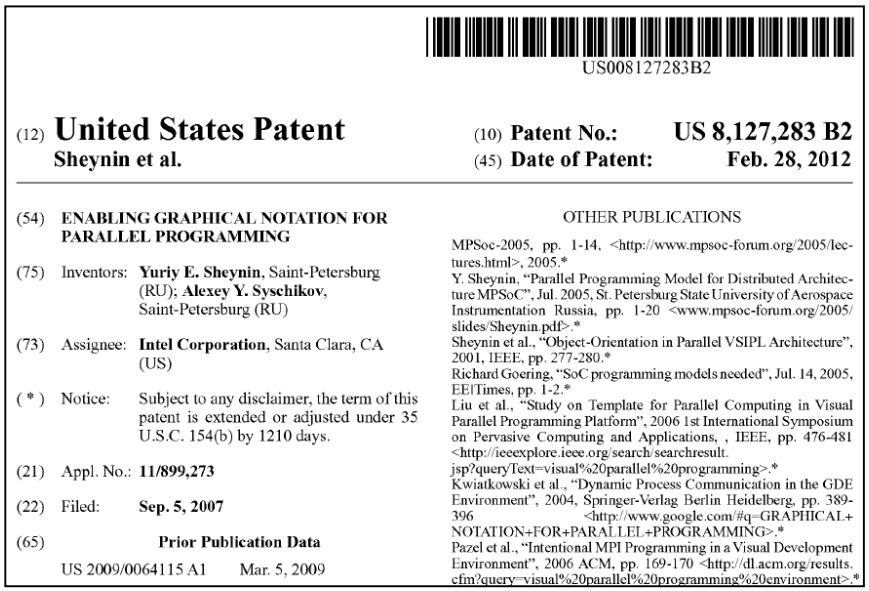
Systems, technologies and tools for portable software development for Embedded Systems



Technology in international collaboration

The technology has a long history and valuable international cooperation.

- Early aspects for multicore/manycore programming were submitted in 2009 to **US patent** together with Intel corp., patent US8127283 was received in 2012
- Technology is applied in **EU Technology Platform** ARTEMIS
  - Project PaPP: Portable and Predictable Performance on Heterogeneous Embedded Manycores
  - Project proposal FOG 2.0: New generation fog computing for intelligent high-performance smart devices



US008127283B2

(12) **United States Patent**
Sheynin et al.

(10) **Patent No.: US 8,127,283 B2**
(45) **Date of Patent: Feb. 28, 2012**

(54) **ENABLING GRAPHICAL NOTATION FOR PARALLEL PROGRAMMING**

(75) Inventors: **Yuriy E. Sheynin**, Saint-Petersburg (RU); **Alexey Y. Syschikov**, Saint-Petersburg (RU)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1210 days.

(21) Appl. No.: **11/899,273**

(22) Filed: **Sep. 5, 2007**

(65) **Prior Publication Data**

US 2009/0064115 A1 Mar. 5, 2009

OTHER PUBLICATIONS

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Sheynin et al., "Object-Orientation in Parallel VSIPL Architecture", 2001, IEEE, pp. 277-280.*
Richard Goering, "SoC programming models needed", Jul. 14, 2005, EEITimes, pp. 1-2.*
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Kwiatkowski et al., "Dynamic Process Communication in the GDE Environment", 2004, Springer-Verlag Berlin Heidelberg, pp. 389-396 <http://www.google.com/#q=GRAPHICAL+NOTATION+FOR+PARALLEL+PROGRAMMING>.*
Pazel et al., "Intentional MPI Programming in a Visual Development Environment", 2006 ACM, pp. 169-170 <http://dl.acm.org/results.cfm?query=visual%20parallel%20programming%20environment>.*

Joint Technology Initiatives - Collaborative Project (ARTEMIS)

ARTEMIS-2011-1

Grant Agreement Number 295440

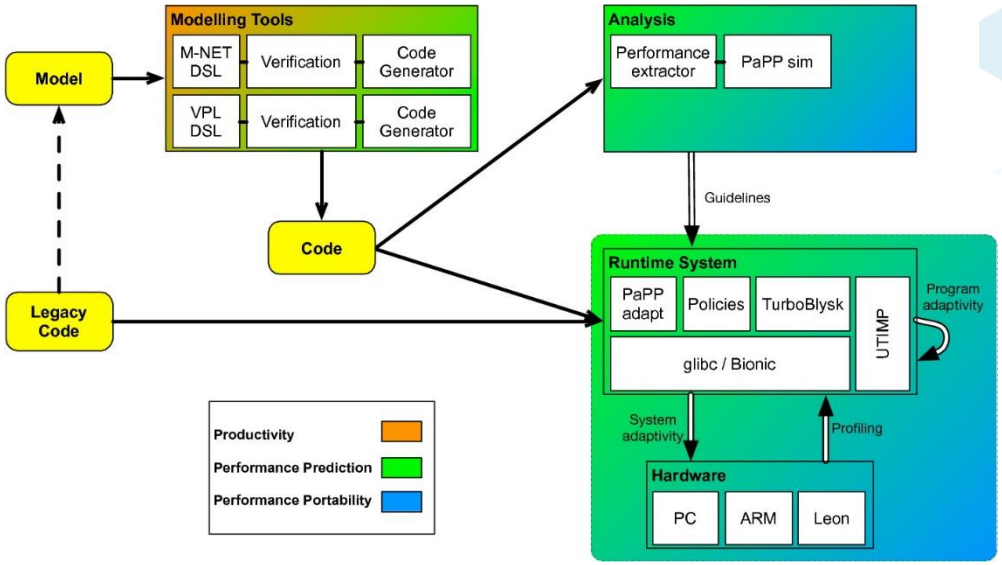
PaPP

Portable and Predictable Performance on Heterogeneous Embedded Manycores

PaPP: Portable and Predictable Performance on Heterogeneous Embedded Manycores

- ARTEMIS project (2012 - 2015)
- 16 organizations from 8 countries
- Project coordinator SICS, Sweden

- **Predictable** and **portable** performance, for
- **Parallel applications**, on
- **Heterogeneous embedded manycores**



Aimed to support cost-efficient development of embedded multicore systems with low time-to-market and hardware costs

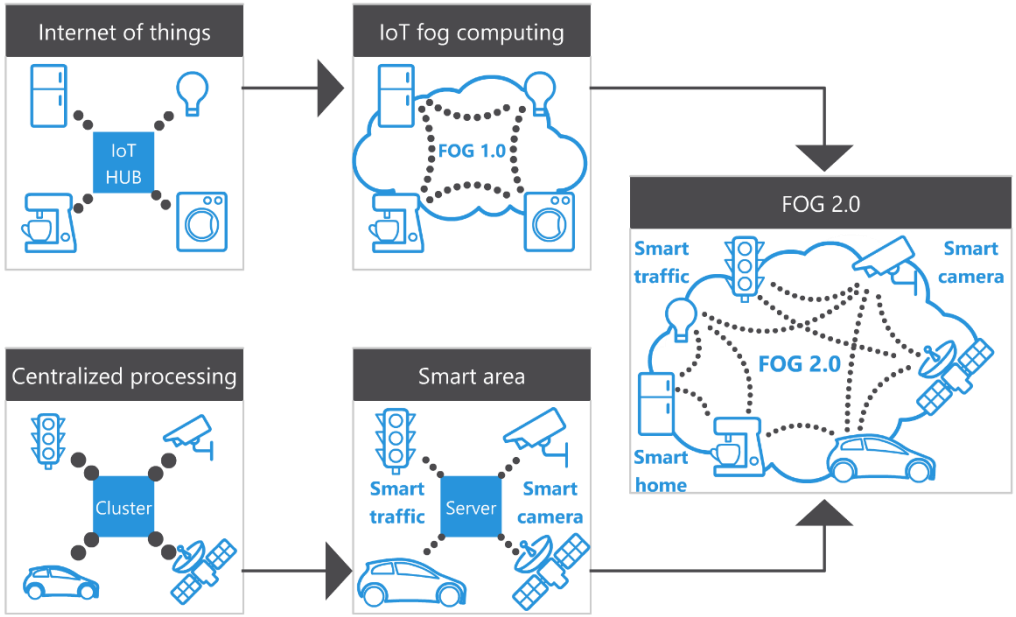
- Achieve performance predictability and portability for configurable and future parallel platforms
- Increase software development productivity

FOG 2.0 - New generation fog computing for intelligent high-performance smart devices

ECSEL Joint Undertaking Call 2017
Electronic Components and Systems for European Leadership

Fog computing developed to enable distributed computations directly between thousands of IoT devices. But the fog computing approach is not suitable for evolving high-performance smart devices.

FOG 2.0 aims to develop applications, hardware, networking and computing distributed infrastructure for next generation distributed smart systems with high-performance embedded platforms based on principles of fog computing.



- Smart Mobility
- Smart Society
- Smart Energy
- Smart Health
- Smart Production

Advance smart applications with FOG 2.0

System-level software

Working on all levels of system software:

Embedded real-time OS

- Developed by SUAI
- Real-time executive
- Portable
- Scalable
- Light-weight

- Embedded SW for SpaceWire switches

Embedded real-time services

- Linux-based
- Real-time services
- Protocols support
- Time services
- Data control

- Processing modules

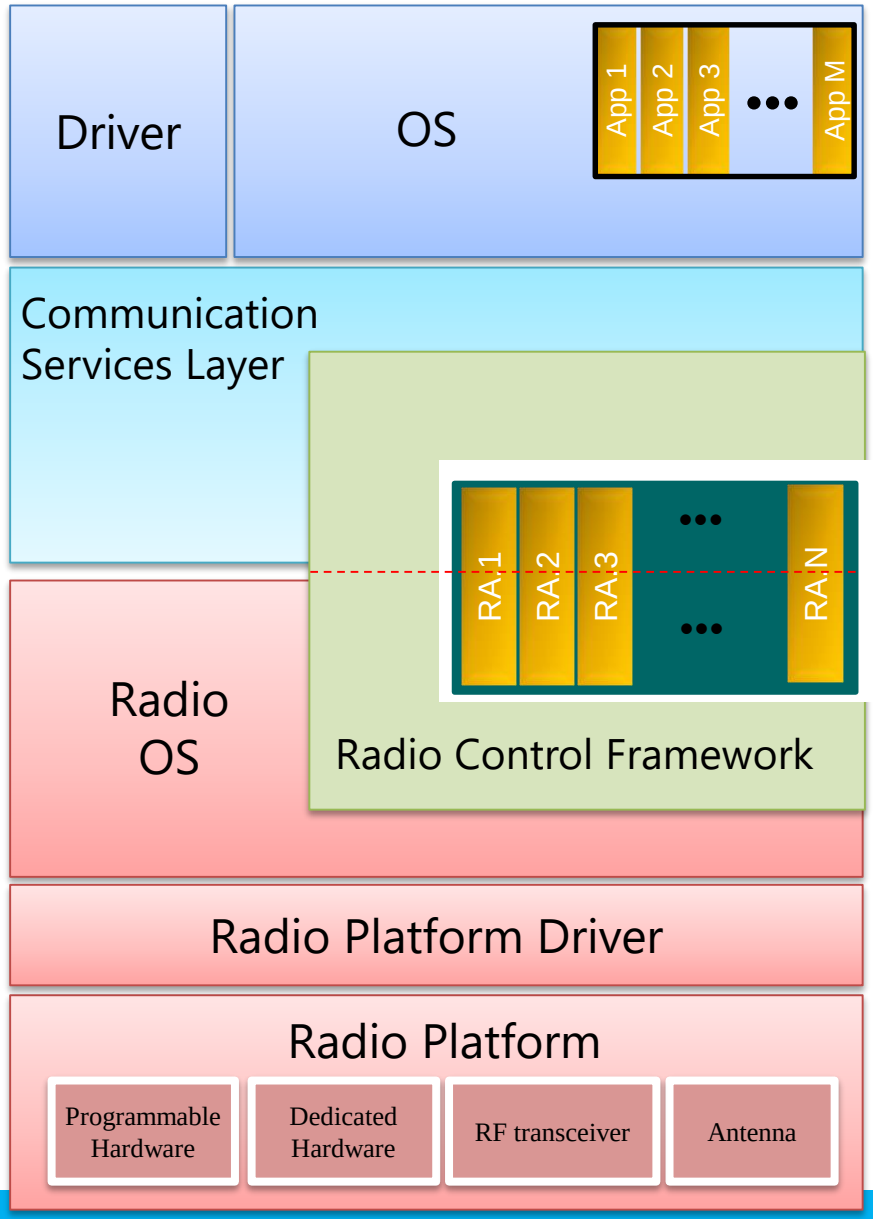
OS with strict partitioning

- Available at partners
- Under investigation by SUAI

- SW for aerospace and automotive systems

Reconfigurable Radio Systems

ETSI EN 303 xxx – European Standard. New (year 2016)!



Multiradio Interface (MURI)

- ✓ Administrative Services
- ✓ Access Control Services
- ✓ Data Flow Services

Unified Radio Application Interface (URAI)

- ✓ Radio Application Management Services
- ✓ User Data Flow Services
- ✓ Multiradio Control Services

Reconfigurable RF Interface (RRFI)

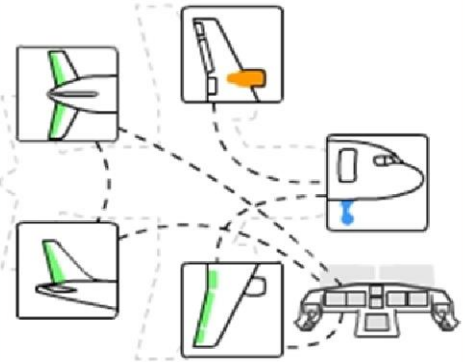
- ✓ Spectrum Control Services
- ✓ Power Control Services
- ✓ Antenna Management Services
- ✓ Tx/Rx Chain Control Services
- ✓ RVM Protection Services

Radio Virtual Machine (RVM)

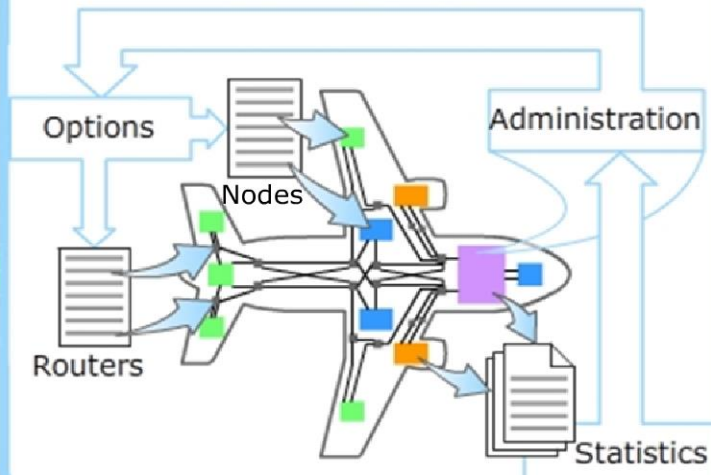
- ✓ Unified Radio Applications model
- ✓ Radio Applications portability
- ✓ Updatable Radio Serivces

System design technology of an on-board computing network for a distributed complexes of airborne equipment

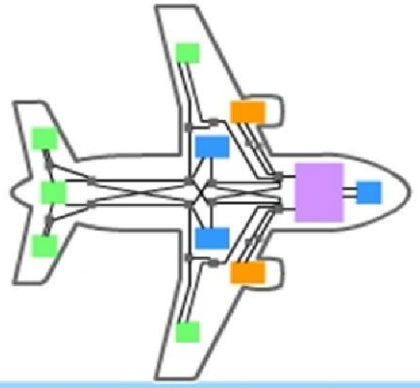
Architecture design



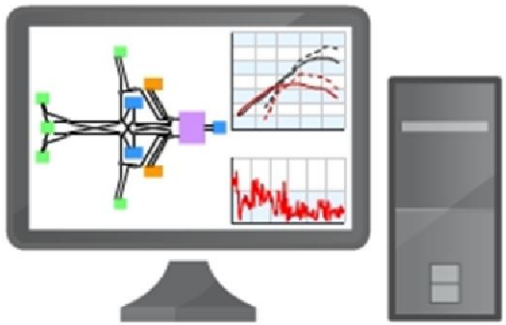
On-board network administration during exploration



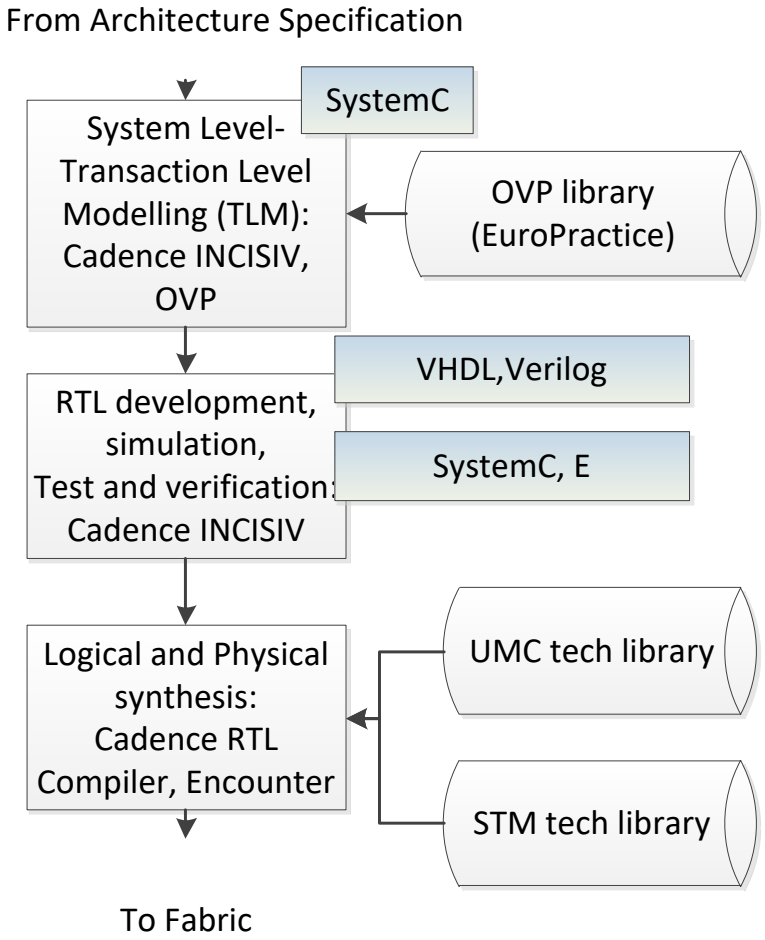
Structure and info-logical configuration design



Distributed on-board network modeling



Hardware development activities
System-on-chip, Network-on-chip design flow



Interface controllers

- SpaceWire
- GigaSpaceWire
- SpaceFibre

Data routers

- SpaceWire / GigaSpaceWire
- SpaceFibre

Controllers

- RMAP
- STP

Data flow hub with stream data preprocessing "on the fly"

These IP-Blocks are silicon and production proved as part of chips on 250 nm, 180 nm, 120 nm tech libraries

Chipset with SpaceWire for aerospace applications (1)

1892VM14YA

System on a chip Multicom-02

Dual-core CORTEX-A9

Dual-core DSP ELcore-30M

2 SpaceWire ports

ECSS-E-50-12C standard

Speed up to 696 Mbit/s

1892VM7YA

Digital signal processor

MIPS32 compatible CPU

Quad-core DSP ELcore-28

2 SpaceWire ports

Speed up to 300 Mbit/s

1892VM15AF

Radiation tolerant signal processor

MIPS32 compatible CPU

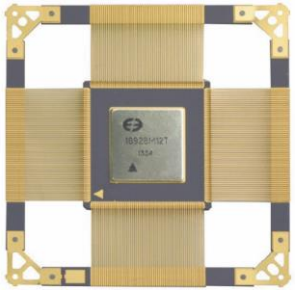
Dual-core DSP ELcore-30M

2 SpaceWire ports

ECSS-E-50-12C standard

Speed up to 300 Mbit/s

1892VM12AT



Radiation tolerant microprocessor

MIPS32 compatible CPU

2 SpaceWire ports

ECSS-E-50-12C standard

Speed up to 300 Mbit/s

Chipset with SpaceWire for aerospace applications (2)

1892VK016

Solid state drive network controller

2 MIPS32 compatible CPUs

2 SpaceWire ports

ECSS-E-50-12C standard

Speed up to 300 Mbit/s

4 ports

SpaceFibre / GigaSpaceWire (SpaceWire-RUS)multiprotocol switch

Throughput up to 1,25 Gbit/s

1892KP1YA

Radiation tolerant SpaceWire switch

Embedded CPU

16 SpaceWire ports

ECSS-E-50-12C standard

Speed up to 200 Mbit/s

1892XD4F (MCV-03R)

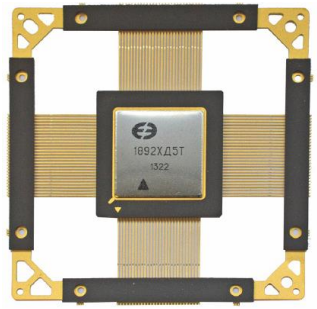
Radiation tolerant multi-channel adapter

4 SpaceWire ports

ECSS-E-50-12C standard

Speed up to 300 Mbit/s

1892XD5T



Radiation tolerant remote RMAP controller

2 SpaceWire ports

ECSS-E-50-12C standard

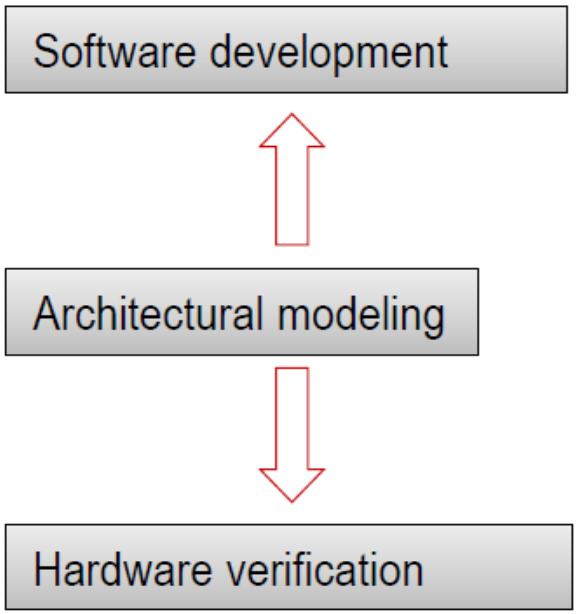
Speed up to 300 Mbit/s

Transaction Level Modeling

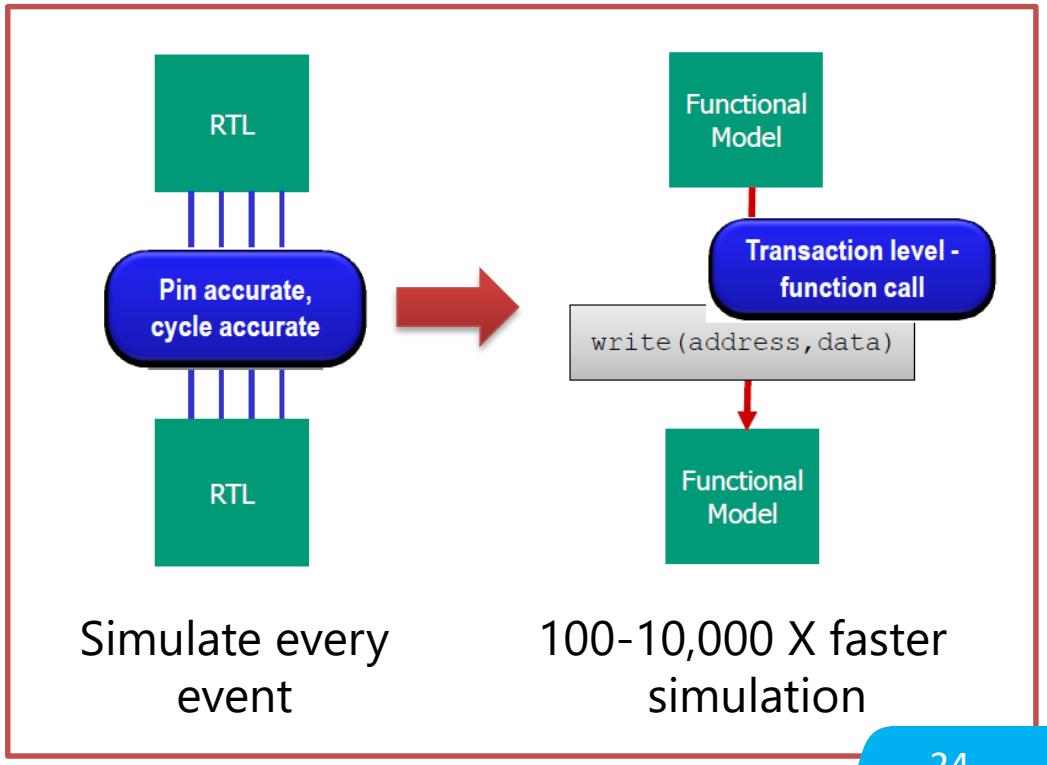
The TLM-2.0 transaction level modeling standard from the Open SystemC Initiative (OSCI):

- Represents key architectural components of hardware platform
- Architectural exploration, performance modeling
- Software execution on virtual model of hardware platform

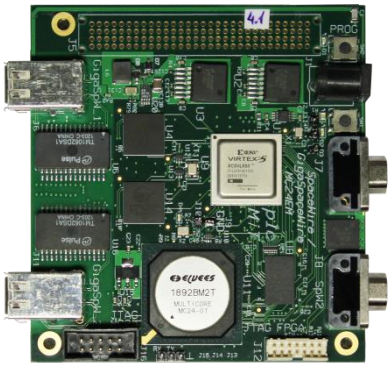
Accelerates product release schedule

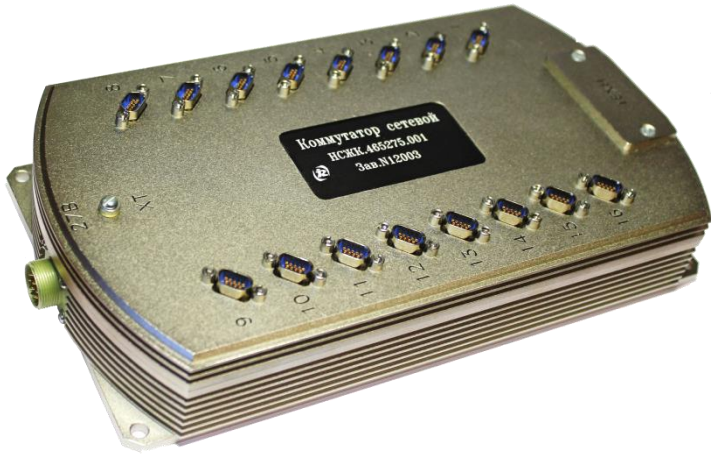


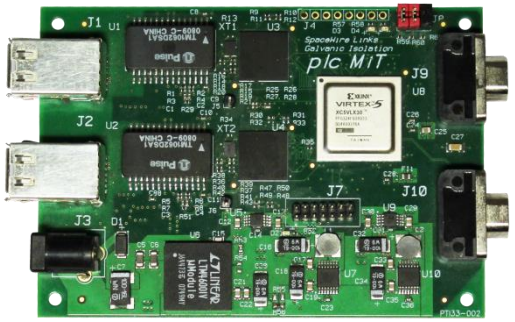
TLM = golden model



Pre-production samples of SpaceWire network system components







MC-24EM module

- SpaceWire and GigaSpaceWire ports
- Running Linux
- TCP/IP stack over SpaceWire

MCK-01, 02 router

- 16-channels SpaceWire router
- Routing on the speed up to 400 mbit/s
- Avionics form factor

SW-GigaSW bridge

- Processorless or with RISC core
- Connects SpaceWire and GigaSpaceWire networks

Main industrial partners

- **ELVEES RnD Center** (*microelectronics production*)
- **Rocket and Space Corporation Energia after S.P. Korolev** (*Space corporation*)
- **The Institute of Aircraft Equipment** (*Aviation company*)
- **JSC "Academician M.F. Reshetnev "Information Satellite Systems"** (*Satellite corporation*)